UNIVERSITI PUTRA MALAYSIA

MODELLING AND SIMULATION OF Si/SiGe HETEROSTRUCTURE DEVICES

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By

NORULHUDA BT ABD. RASHEID

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of Requirement for the Degree of Master of Science

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To my beloved family

my husband, Mohd Radhwan Abd Karim
and my children, Farisa Alia, Muhammad Farhan and Ili Rawaida.

Thank you for giving me the full support and confidence through out my studies
and most of all thank you for giving me all the LOVE I need.

May ALLAH bless you all... .....Amin

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirements for the degree of Master of Science

MODELLING AND SIMULATIONS OF THE Si/SiGe HETEROSTRUCTURE DEVICES

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NORULHUDA BT ABD RASHEID

April 2002

Chairperson: **Roslina bt Mohd Sidek, Ph.D.**

Faculty: **Engineering**

Complementary metal-oxide-semiconductor (CMOS) is currently the most dominant technology used in making integrated systems. It consists of both n-channel MOS transistor (NMOS) and p-channel MOS transistor (PMOS) fabricated on the same substrate. Conventionally, the substrate is made of silicon. Alternatively, the substrate can be made from different layer of semiconductors known as heterostructure. Much attention has been given to Si/SiGe due to its compatibility with silicon and the higher carrier mobilities. SiGe is an alloy which is said to be an alternative solution to the problem of a down-scaled CMOS to produce high speed device.

This work consists of modelling three different of Si/SiGe heterostructure substrates which are used to construct n- and p-channel MOSFETs and later to construct CMOS inverter. The three types of heterostructures are a strained SiGe on silicon substrate, a strained silicon on relaxed SiGe/Si substrate and a strained SiGe on strained Si/relaxed layers of SiGe/Si substrate.

A device simulator, Avanti MEDICI Version 1999.2 is used in this project. Although it has heterojunction capability, it does not support model for a strained Si. This work also highlights the method to simulate Si/SiGe heterostructures containing strained layer using MEDICI. Simulations on the band structure and current-voltage (I-V) characteristics of the MOSFETs are carried out. The I_d-V_g and I_d-V_d are simulated for different value of Ge% and mobility. This is to observe the effect of varying the value of Ge% and mobility used in the design. The simulation on the CMOS inverter as the fundamental circuit is carried out to obtain the transfer curve. The noise margin and switching characteristics can be extracted from the transfer curve.

All the simulated results are then compared with the Si bulk. The analyses show that the performance of the Si/SiGe heterostructures is better in terms of the electrical characteristics of the MOSFETs and the switching characteristics of the CMOS inverter, as compared to the performance of the Si bulk.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

MODEL DAN SIMULASI PERANTI-PERANTI SIMPANG-HETERO Si/SiGe

Oleh

NORULHUDA BT ABD RASHEID

April 2002

Pengerusi: **Roslina bt Mohd Sidek, Ph.D.**

Fakulti: **Kejuruteraan**

Semikonduktor-oksida-logam pelengkap (CMOS) adalah teknologi dominasi terkini dalam membuat sistem bersepadu. Ia terdiri daripada transistor MOS saluran n (NMOS) dan transistor MOS saluran p (PMOS) yang difabrikasikan di atas substrat yang sama. Kebiasaannya, substrat diperbuat daripada silikon. Secara pilihan, substrat boleh juga dibuat daripada lapisan semikonduktor yang berlainan yang dikenali sebagai struktur-hetero. Perhatian yang banyak telah diberikan kepada struktur-hetero Si/SiGe kerana keserasiannya dengan silikon dan mobiliti-mobiliti pembawa yang tinggi. SiGe adalah sejenis aloi yang dikatakan sebagai salah satu penyelesaian terhadap masalah pengecilan CMOS dalam menghasilkan peranti yang berkelajuan tinggi.

Projek ini mengandungi pemodelan tiga jenis struktur-hetero Si/SiGe yang akan digunakan untuk membina saluran n dan p dan kemudian untuk membina pembalik CMOS. Tiga jenis struktur-hetero tersebut adalah SiGe tegang di atas substrat silikon, silikon tegang di atas lapisan rehat SiGe/substrat Si dan SiGe tegang di atas lapisan silikon tegang/lapisan-lapisan rehat SiGe/substrat Si.

Alat simulasi peranti, Avanti MEDICI Versi 1999.2 digunakan untuk mensimulasikan struktur jalur dan ciri-ciri arus-voltan MOSFET. Walaupun mempunyai keupayaan simpang-hetero, ia tidak menyokong model untuk silikon tegang. Cara-cara untuk mensimulasikan struktur-hetero Si/SiGe yang mempunyai lapisan silikon tegang dengan menggunakan MEDICI diketengahkan di dalam tesis ini. Simulasi dijalankan ke atas struktur jalur dan ciri-ciri arus-voltan (I-V) MOSFET. I_d-V_g dan I_d-V_d disimulasikan bagi nilai Ge% dan mobiliti yang berbeza. Ini adalah bertujuan untuk memerhati kesan perubahan nilai Ge% dan mobiliti dalan rekabentuk tersebut. Simulasi ke atas pembalik CMOS sebagai litar asas dijalankan untuk mendapatkan lengkung pindah. Jidar hingar dan ciri-ciri suis boleh didapati daripada lengkung pindah tersebut.

Keputusan-keputusan simulasi kemudian dibandingkan dengan Si pukal. Analisis-analisis menunjukkan bahawa pencapaian bagi simpang-hetero Si/SiGe adalah lebih baik jika dibandingkan dengan pencapaian bagi Si pukal, dari segi ciri-ciri elektrik MOSFET dan ciri-ciri suis pembalik CMOS.

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Other deserving thanks include Norhazlin bt Jalalludin, the research assistant to Dr. Roslina, who has taught me to use the device simulator, MEDICI. Also, I would like to thank the other supervisory committee members, Encik Rahman Wagiran and Encik Nasri for the valuable comments and guidance.

I certify that an Examination Committee has met on 22nd April 2002 to conduct the final examination of Norulhuda bt Abd. Rasheid on her Master of Science thesis entitled "Modelling and Simulations of Si/SiGe Heterostructure Devices" in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulations 1981. The Committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committee are as follows:

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This thesis submitted to the Senate of Universiti Putra Malaysia has been accepted as fulfilment of the requirement for the degree of Master of Science.

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DECLARATION

I hereby declare that the thesis is based on my original work except for equations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

(NORULHUDA BT ABD. RASHEID)

Date: 2 Mei 2002

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LIST OF ABBREVIATIONS

MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MESFET	Metal-Semiconductor Field Effect Transistor
MODFET	Modulation-Doped Field Effect Transistor
NMOS	n-channel Metal-Oxide-Semiconductor
PMOS	p-channel Metal-Oxide-Semiconductor
CMOS	Complementary Metal-Oxide-Semiconductor
SiGe	Silicon-germanium
V_T	Threshold voltage
I_{Dsat}	Saturated drain current
μ_e	Electron mobility
μ_h	Hole mobility
E_g	Energy gap
E_V	Valence band energy
E_C	Conduction band energy
V_{dd}	Supply voltage
I-V	Current-voltage
NM_L	Low noise margin
NM_H	High noise margin
V_{IH}	High input voltage
V_{IL}	Low input voltage
V_{OH}	High output voltage
V_{OL}	Low output voltage

CHAPTER 1

INTRODUCTION

Complementary metal-oxide-semiconductor (CMOS) consists of both n-channel MOS (NMOS) and p-channel MOS (PMOS) transistors fabricated on the same substrate as shown in Figure 1.1 [1].

Since the early eighties until today, complementary metal-oxide-semiconductor (CMOS) has emerged as the dominant technology for general purpose integrated circuit applications [2]. As trend continues, CMOS has edged out less competitive technologies such as bipolar and NMOS, while relegating more exotic technologies such as GaAs to niche applications.

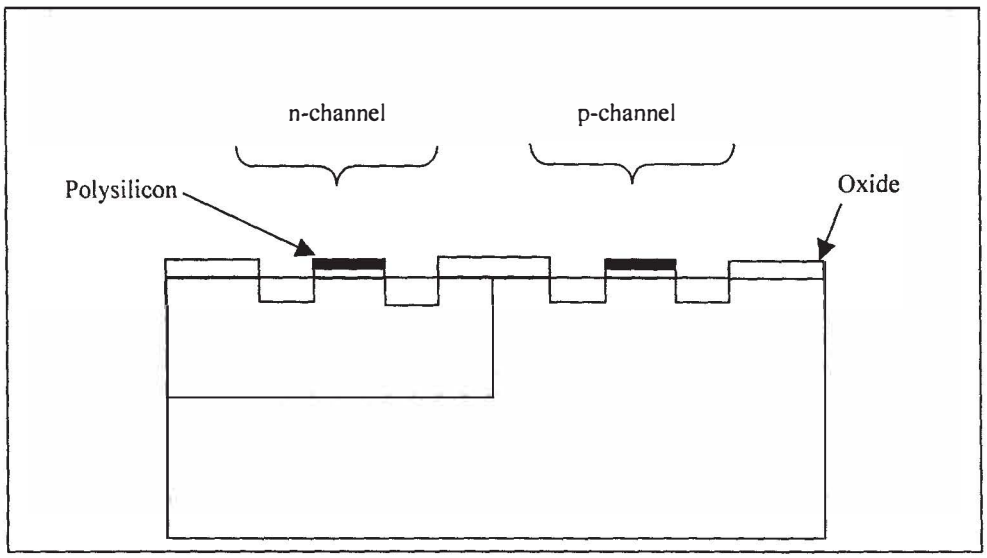

Figure 1.1: Cross-section of CMOS

1.1 The Advantage of CMOS

CMOS is recognized as a leading contender for existing and future VLSI systems. Since the beginning of VLSI era, CMOS technology has gained more and more significance than its predecessor: the NMOS technology. There are several main reasons, which has contributed to the use and acceptance of the CMOS technology [3]. CMOS circuits have been at the forefront of the technology primarily due to their passive power consumption. Aside from leakage currents, power in digital circuits are dissipated only during switching events. There is virtually no power consumed when the circuit is in steady state.

Another significant feature of CMOS is its stability of operation. Unlike its counterpart technologies such as NMOS and bipolar, small deviation in device characteristics do not perturb the circuit operating point. It has proven to be robust and permits large quantities and varieties of ICs to be fabricated with high yield.

CMOS is flexible for a wide variety of applications, which includes digital logic, static/dynamic random access memories (RAMs), signal processing and a variety of analogue circuits. As a result, CMOS technology has reached the enviable position where supply generates its own demand. The wide applicability of CMOS has given rise to a broad, high quality infrastructure for development and fabrication that allows advances to be made widely available at a reasonable cost.

In the CMOS circuit, the p-channel transistor has lower performance compared with

n-channel transistor because of the lower mobility of holes than the electrons. However, the performance difference between PMOS and NMOS has reduced drastically due to velocity saturation thus making CMOS technology more attractive in VLSI circuit. CMOS also has another advantage, which is a very large noise margin [4].

1.2 Limitations of Down-Scaled CMOS

From 1960's until now, speed improvement is achieved through down scaling. There are some physical limitations due to down scaling such as the gate oxide becomes very thin (~ 30 Å), the source and drain resistances become more dominating and other parasitic effects. This will reduce the reliability of the device. This is where SiGe alloy is introduced as an alternative solution to produce high speed device.

1.3 Silicon Germanium (SiGe)

A few years after the invention of the bipolar transistor the basic electronic semiconductor material changed from germanium to silicon. During that switch around 1960 considerable interest was focused on bulk, unstrained SiGe alloys. Advance epitaxy methods have enabled the growth of high quality, thin, strained SiGe layers on Si substrates since around 1985 [5]. The availability of strained SiGe/Si structures stimulated heavily the research on silicon-based heterostructure devices resulting within a few years in the fastest silicon-based transistors and other very attractive options.

1.4 The Advantage of Si/SiGe

There have been suggestions to use complementary heterostructure field-effect transistors based on GaAs/AlGaAs in order to make use of the high electron mobility in this material system [6]. However, the problem of the low mobility which plagues Si was not solved. In addition, that technology relied on making Schottky gates, which result in several orders of magnitude higher gate leakage current than in oxide-gated devices.

Unlike the other group III–V elements (e.g. GaAs), SiGe is compatible with silicon process. The intrinsic advantage of Si/SiGe allowing the high-speed operation of the transistors at lower supply voltage would, in principle, result in higher reliability. Although it is inconceivable that Si/SiGe Heterojunction CMOS (HCMOS) will replace Si CMOS in ULSI applications in the near future, there is increasing interest in application-specific designs which require low power consumption and high speed (e.g., cellular phones, other portable electronics, opto-electronic receivers, etc.) [6]. This is where we believe that there is ample room for implementing Si/SiGe HCMOS, making use of its potential performance leverage over Si CMOS.

If cryogenic applications become of importance, the advantage of Si/SiGe over Si will become even more clear, since at 77 K for instance, the electron and hole mobilities are an order of magnitude higher than in Si.